Amendments to the Specification

Please amend paragraph [0040] of the specification as follows:

[0040] It is noted here that, as part of the DLL calibration process, while each pair of victim and aggressor patterns is present on the corresponding bit lines in the data bus 18, the processor 14 (FIG. 1) performs a test data write/read operation (block 66 in FIG. 3) on the memory cells 26 with the help of the memory controller 32. Based on the accuracy or integrity of the data read during various data write/read operations, the processor 14 (preferably, the memory controller 32) may adjust the value of the delay programmed in the DLL 40 (as shown in block 67 in FIG. 3) to be applied to the strobe signals from the strobe generation circuit 38. The programming of the DLL may be referred to as "DLL calibration." As is known in the art, the process of DLL calibration typically involves reading memory data relative to the memory controller 32; the data is written and then read back with a middle DLL setting for the data receiving strobe. The data read is then checked for errors against the data written. This process may be repeated with various DLL settings until an error is found at the longest/highest delay setting and at the lowest/shortest delay setting. The DLL may be then set or "calibrated" in the middle of these two settings. This process could also be applied to data writes using a DLL on the transmit/write strobe. A detailed description of how a DLL may be calibrated can be found in the U.S. Pat. No. 6,401,213 to Jeddeloh, the disclosure of which is incorporated herein by reference in its entirety.